# Frequency Analysis Method for Propagation of Transient Errors in Combinational Logic

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## Abstract

*The continuous development of VLSI technology is shrinking the minimal sizes to nanometer region, making circuits more susceptible to transient error. In this paper, we present a frequency analysis method to accurately estimate the possible propagation of transient fault-due glitches through a CMOS combinational circuit. We use the frequency feature of signal and frequency response of electrical system to analyze the propagation of transient error. Experiments show that on average, our approach provides approximately 95% accuracy and several orders of magnitude faster with respect to HSPICE simulation.*

## 1. Introduction

Technology scaling down leads to the smaller feature size, lower power supply and higher clock frequency. The trend of technology makes circuits on chip more complex and faster, at the same time, more susceptible to the compound noises, such as cross-talk, ground bounce, substrate coupling noise and radiation induced noise like soft error. While soft error has become an unavoidable problem in microelectronics, the estimation of the soft error rate (SER) of a circuit attracts more attention because conventional methods, which depend on HSPICE to analyze the SER of circuits, are slow in simulation and not applicable to the very large circuits. It becomes emergent for researchers to contribute faster and more accurate methods for SER estimation.

With the continuous advances in microelectronics technology, recent study[1] shows that SER in combinatorial logic will come to an important place as memory units in 2011. Traditionally, combinational logic is being considered non-sensitive to soft error dues to three factors: logic masking, electrical masking and latch window masking. Among the three masking features, electrical masking is the most difficult to estimate. Therefore, intensive research has been devoted to the analysis and modeling of transient fault [2][13][4][5]. In [2], they studied the propagation of transient fault among the combinatorial logic according to the height and the duration of transient fault. In their studies, they found that there are three intervals of input glitch durations which can results in attenuation propagation of the glitch. In [11] , they proposed a method using table lookup MOSFET models to capture the nonlinear properties of submicron MOS transistor. Furthermore, they proposed two methods to calculate the pulse propagation by table lookup. In [12], simple RC model is proposed to solve this problems. In [13][14][15], equivalent inverter based approaches are proposed to the propagation of transient fault. In summary, although extensive research work has been done, few have tried to analyze the propagation of transient fault in combinatorial logic by frequency method and provide a precise model.

Frequency method has usually been used to analyze the linear system. But in the digital circuits, frequency methods have seldom been used to analyze the signal because transistor is composed of three linear regions, saturation region, amplify region and cut-off region. In fact, the energy of transient fault is not strong enough to pass through active region and drive the transistor to work at the saturation region or cut-off region. The transistor is working at one linear region in the most time. It is a good choice to use frequency method to analyze the electrical masking in combinatorial logic because most transient error glitches are high frequency and weak in signal energy.

In our paper, we present a frequency analysis method to accurately estimate the possible propagation of transient fault-due glitches through a

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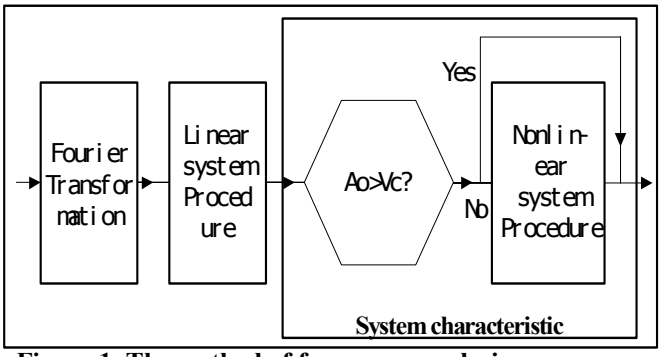


**Figure 1. The method of frequency analysis**

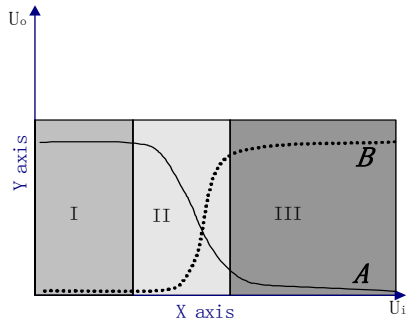


**Figure 2. Transfer features of transistor**

combinational circuit. This paper is organized as follows. In section 2, the frequency method is introduced in detail. In section 3, the experimental results are reported. Finally we conclude the paper in section 4.

## 2. Frequency Analysis Method

In our approach, we try to estimate the propagation of the transient fault in frequency domain. According to [11], we can calculate the output of one linear system by multiply the frequency expression of the input signal and the frequency features of the linear system. Our approach includes two methods, which depend on the energy of transient error.

(1) One is for a transistor working at the region II (amplify region) as shown in Figure 2. An electrical system is a linear system while the transistor is working at region II. According to [10], the output of linear system can be calculated if the frequency feature of the input and the electrical system is given.

(2) The other is for an electrical system that is working at the region III. It becomes complicated when the electrical system is a nonlinear system, which can not be calculated directly by method one. Method two is divided into two steps as shown in Figure 1. The first step is a linear procedure which is same to the method one, while the second step is a nonlinear procedure which handles the difference features between two regions ( region II and region III ). In the nonlinear procedure, there is a critical value of magnitude of signal Vq, which is critical to decide the electrical system's working region. If the magnitude of the basic element is beyond the critical value, the electrical system is working at the region III. The nonlinear system is specially designed to handle the magnitude of a signal which is over the critical value.

We can use Fourier transformation and frequency response of a linear system to calculate the output of an electrical system. The frequency response of circuits in one Cell library is abstracted by HSPICE model. Finally, we can calculate the final result of one circuit through our algorithm.

In a VLSI chip, there are many electronic nodes. It will be very complicated to calculate the propagation of a glitch in combinatorial logic. In practice, there are two approaches to this problem. In the first approach, the path of one circuit is regarded as a whole system. In the second approach, the path of one circuit is regarded as the linkage of different subsystems. We prefer the second approach in our work.

### 2.1 Fourier Transformation of A Glitch

#### 2.1.1 Accuracy at Number of Harmonic Elements

At the first step of our approach, a glitch should be decomposed into summation of different frequencies of sinusoidal functions by Fourier transformation. It should be serious to consider how many harmonics elements are necessary to reach high accuracy. We analyze the relationship between the numbers of harmonic elements and the accuracy achieved. Approximately 90% of accuracy can be achieved when a glitch is decomposed into three harmonic elements. If we want to achieve up to 97% accuracy, more than nine harmonic elements should be considered

#### 2.1.2 The Constant of Fourier Expression

In this section, we will introduce how to wipe out of the constant of Fourier expression. The glitch of transient error is a periodic signal which can be expressed by Fourier series equation, as shown at 1), where $A_0$ is the constant in the expression. The constant at a mathematical equation means to the quiescent point in an electronic circuit, which is a major parameter of the frequency response function.

As shown in Figure 3, we divide a glitch into two parts according to its magnitude. One part is 90% of the magnitude of signal voltage and the other part is 10% of the magnitude of voltage. We turn the shadow part of the glitch into another side of X-axis, and expand the cycle of the glitch into 2*t. Because the signal is symmetry from the X axis, the constant of the equation is smoothed away.



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$$x(t) = A_0 + A_1 \sin(wt) + A_2 \sin(2wt)... \quad 1)$$

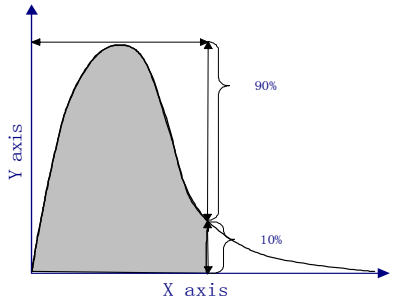


**Figure 3. Division of a glitch**

### 2.2 Linear System Procedure

In our approach, a linear system means that the transistor works at region II. The frequency response of one electrical system depends on the quiescent point of circuit, as shown in Figure 4. We analyze the accuracy of the frequency calculation when different quiescent point of one circuit is given. In the experiment, 65nm INV circuit is used. In Figure 4, we can conclude that when a system works at region II, 10% of voltage would be the better choice to calculate the frequency response in the linear system procedure.

### 2.3 Nonlinear System Procedure

In our approach, a transistor may cross two linear system (from region II to region III) when the magnitude of the signal is high enough. So, the nonlinear system procedure is necessary to handle this case. The major part of our nonlinear system procedure is the input-output function 2) and 3), which can be retrieved from the HSPICE simulation.

$$Y=a-a * \arctan(b*(x-c)) /(\pi*0.5) \quad 2)$$

$$Y=a+a * \arctan(b*(x-c)) /(\pi*0.5) \quad 3)$$

In the above equations, the magnitude of the output voltage is two times of a. b is the parameter which is decided by the specific cell library. c is the middle voltage of input signal when the system is working at amplify region.

### 2.4 Gate as a Subsystem

In a VLSI chip, there are many gates on one path. In practices, we regard every gate as one subsystem. Before calculation, subsystem characteristics would be retrieved and the characteristics can be reused in the calculation of another path. After the characteristic of one cell library is extracted, parameters can be used on all circuits mapped to the same library. This reusable system characteristics will be time saving in calculation.

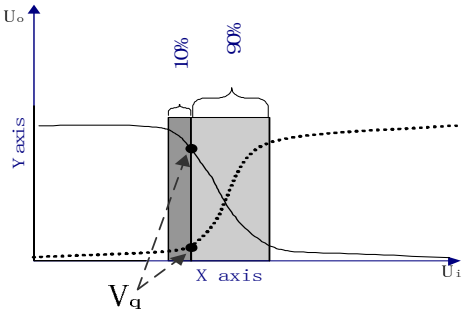


**Figure 4. Input-Output feature of a transistor**

But increase of electrical nodes in one path will lead to the loss of more accuracy.

## 3. Experiments and Results

A computer program is designed to realize our approach. The program is accomplished by C computer language. In our experiment, ISCAS'85 benchmark circuits are analyzed. All circuits were implemented in 65nm process technology using scaled MOSIS layout design rules. The calculation result has been compared with the result from HSPICE simulation. These simulation and calculation is performed on PC platform with Pentium IV CPU 1.8GHz, 640MB memory. And the compiler for C program is VC++ 6.0.

In this experiment, five large circuits in ISCAS'85 are applied. We choose three longest paths of every circuit for evaluation, denoted as Path 1, Path 2, and Path3 in Table I, while Path 1 is the longest. In our analysis, $9^{th}$ harmonics is considered. Four different periods of signals were studied. They are 0.05ns, 0.07ns, 1ns and 1.05ns respectively. Accuracy is used to evaluate the difference between the calculated voltage and that of HSPICE, while average accuracy is the mean accuracy under different periods of signals. Timing saving in Table 1 is the ratio of calculation time of our approach to that of HSPICE.

Experiment result shows that the accuracy degrades as the nodes on a path increase. About 0.12%~0.5% of accuracy would be lost when one node is added in one path. But there are more time can be saved when there are more nodes on a path, as shown in Table 1.

## 4. Conclusion

In this paper, we presented a frequency approach to calculate the propagation of glitch in combinational logic. We use the frequency feature of signal and frequency response of electrical system to analyze the propagation of transient error. Our approach is divided into two steps. One is to calculate the linear property of system and the other is to calculate the nonlinear property. The experimental results showed that accuracy



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of the proposed approach is close to that of HSPICE, but HSPICE is much more time consuming.

**Table 1. Accuracy and time saving**

| Path / ISCAS'85 Ciruits | | Path1 | Path2 | Path3 |
|---|---|---|---|---|
| C432 | Average accuracy | 94.95% | 95.025% | 95.025% |
| | Time saving | 422.5 | 416.9 | 421 |
| C499 | Average accuracy | 94.675% | 95.15% | 95.75% |
| | Time saving | 404.87 | 377.7 | 379.12 |
| C6288 | Average accuracy | 92.675% | 91.9% | 92.375% |
| | Time saving | 1196 | 1193.87 | 1194.2 |
| C880 | Average accuracy | 92.4% | 92.91% | 93.1% |
| | Time saving | 538.67 | 528.7 | 521.6 |
| C1355 | Average accuracy | 92.975% | 93.575% | 93.275% |
| | Time saving | 599.27 | 587.62 | 592.6 |

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